

# High- $\kappa$ field-effect transistor with copper-phthalocyanine

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**Abstract.** The use of  $\text{SrTiO}_3$  dielectrics as high-permittivity insulator in organic thin film field effect transistors (FET) is evaluated. Field-effect transistors with sputtered  $\text{SrTiO}_3$  and copper-phthalocyanine (CuPc) as semiconducting layer were fabricated. The device preparation was performed *in-situ* in an ultra high vacuum chamber system. The dielectric in the transistors had a permittivity of up to 200 which led to low driving voltages of 3 V. The field effect transistors were *p*-type and reached mobilities of about  $\mu = 1.5 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$  and an on/off ratio of  $10^3$ . These properties are compared to devices based on other dielectric materials.

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## 1. Introduction

The gate dielectric plays a crucial role for the functionality of thin film field-effect transistors. It is responsible for the reliability of the device, governs the required driving voltages and also limits the polarizations which can be achieved at the interface. In organic thin film transistors the most common dielectric is  $\text{SiO}_2$ . It is well known and characterized from its use in the conventional semiconductor industry, and has the advantages of excellent insulation with low leakage currents and chemical stability. The required silicon wafers with an oxide dielectric layer are commercially available and the source and drain electrodes can be easily fabricated by lithography or by deposition through a shadow mask. Various groups have in this way prepared transistors with different organic layers such as pentacene or copper-phthalocyanine [1, 2]. This approach allows to concentrate on the growth of the active organic layers, but limits the experiments to the regime of low charge carrier concentrations. Many organic materials show electronic interactions which are strongly influenced by the charge carrier concentration. Examples are charge transfer salts based on organic molecules such as tetrathiofulvalene-tetracyanoquinodimethane (TTF)-(TCNQ) [3, 4, 5] or  $\text{K}^+\text{TCNQ}^-$  [6] which show the behavior of a Peierls or Mott insulator [7]. Large changes in the charge carrier concentration may even induce a Mott metal-insulator transition, allowing for a so called Mott transition field-effect transistor (MTFET) [6, 8]. It is therefore interesting to grow these materials in transistor structures where high polarizations can be reached. But also for other organic semiconductors, where no Mott metal-insulator transition occurs, the utilization of high kappa dielectrics is interesting, because the high polarizations result in transistors with low driving voltages.

The charge carrier concentration at the insulator surface which can be induced in field-effect experiments is the product of breakdown field and dielectric constant evaluated at the breakdown field [9]. It therefore depends on the intrinsic properties of the material. With  $\text{SiO}_2$  as dielectric a breakdown field of  $E_{BD} = 10 \text{ MV cm}^{-1}$  and polarizations of up to  $3 \mu\text{C cm}^{-2}$  are possible at best, while with complex oxide dielectrics with a perovskite structure polarizations in the range from  $10 - 40 \mu\text{C cm}^{-2}$  can be achieved under carefully optimized conditions [10].

## 2. Materials

From the perovskite class  $\text{SrTiO}_3$  is one of the best characterized materials. It has a cubic crystal structure with a lattice constant of  $a = 3.905 \text{ \AA}$  and the advantage of a high dielectric constant of  $\epsilon_r = 300$  for bulk material at room temperature. Thin films of  $\text{SrTiO}_3$  have been grown with various techniques, such as RF sputtering [11], pulsed laser deposition [12] or molecular beam epitaxy [13]. The dielectric constant and breakdown voltage in thin film samples is in general lower than in bulk samples most likely due to defects and inhomogeneities of the electric field caused by surface roughness [11]. Furthermore,  $\text{SrTiO}_3$  can be doped with niobium, which results in a

conductive crystalline substrate material, ideally suited for the growth of an epitaxial dielectric SrTiO<sub>3</sub> layer [14].

In this work, to demonstrate the capability of SrTiO<sub>3</sub> as high- $\kappa$  dielectric for organic thin film field-effect transistors, the well known organic *p*-type semiconductor copper phthalocyanine was chosen as the active layer. CuPc (CuN<sub>8</sub>C<sub>32</sub>H<sub>16</sub>) is a crystalline synthetic blue pigment from the group of phthalocyanine dyes. It has been used by various groups in field-effect experiments, usually with SiO<sub>2</sub> as the dielectric when deposited as thin films, but also already with high-permittivity insulators [1, 15].

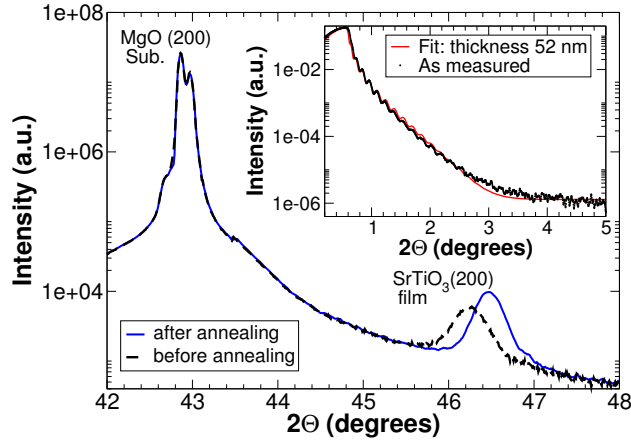
### 3. Device preparation

An ultra high vacuum (UHV) system was employed for the preparation of the devices. It consisted of distinct chambers used for the individual process steps. The growth of the dielectric layer, active layer and the contact preparation was studied separately before they were combined to fabricate field effect transistors completely in-situ.

#### 3.1. SrTiO<sub>3</sub> sputtering

For the growth of the SrTiO<sub>3</sub> layers RF-sputtering was used. The growth of sputtered SrTiO<sub>3</sub> was characterized with X-ray diffraction employing Cu-K $\alpha$  radiation in parallel beam mode and optical microscopy and optimized with respect to high crystallinity, a smooth surface and a sufficient growth rate. The sputtering target had a diameter of two inches and was at a distance of about 15 cm from the substrate.

For the final FET structure preparation SrTiO<sub>3</sub> layers had to be grown on Nb-doped SrTiO<sub>3</sub> (100) substrates. Since by X-ray diffraction thin film and substrate related Bragg reflexions can in this case hardly be discriminated, the dielectric layer growth was optimized on MgO (100) substrates. The thus obtained sputtering parameters were then used for FET preparation on Nb-doped SrTiO<sub>3</sub> (100) employing an argon/oxygen mixture of 2:1 at a chamber pressure of 0.025 mbar, a substrate temperature of 720 °C and a forward sputter power of 100 W. The films were post annealed inside the chamber at 890 °C for 1 hour in an oxygen atmosphere of 0.01 mbar. The deposition time was 90 minutes for field-effect transistor preparation which resulted in a nominal thickness of about 450 nm. During the optimization on MgO the SrTiO<sub>3</sub> films grew preferentially in the (100) direction. The Bragg peaks of the sputtered films were shifted to lower  $2\theta$  values as compared to bulk SrTiO<sub>3</sub>. This was probably related to the larger lattice constant of MgO ( $a = 4.216\text{\AA}$ ) as compared to SrTiO<sub>3</sub> ( $a = 3.905\text{\AA}$ ) which caused a tensile stress due to the misfit [16]. Post annealing further improved the crystalline quality of the SrTiO<sub>3</sub> films. This was demonstrated ex-situ in an oven at 800 °C for 24 h, so that the sample properties could be compared before and after annealing. The SrTiO<sub>3</sub> films showed an increase in the height of the Bragg peak and a shift in position in direction of bulk SrTiO<sub>3</sub>, as is exemplarily shown in Fig. 1.

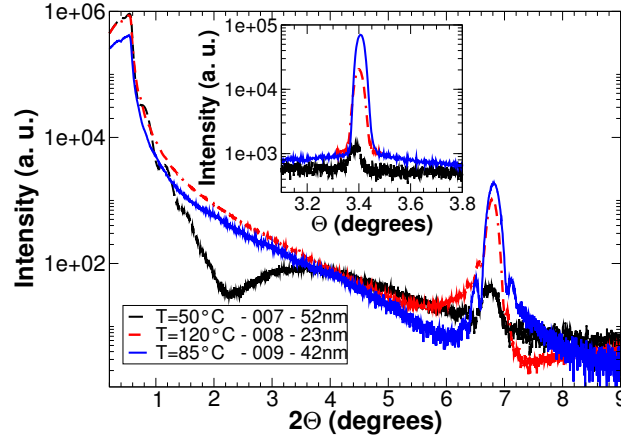


**Figure 1.** (Color online) X-ray scan with the (200) Bragg peak of a sputtered  $\text{SrTiO}_3$  film on a MgO substrate before and after annealing in air. The height of the peak increased and the center shifted toward the literature value for bulk  $\text{SrTiO}_3$  ( $2\theta = 46.472^\circ$ ). Similar behavior was observed for several films. The inset shows the corresponding thickness measurement of the  $\text{SrTiO}_3$  film and a simulated curve to determine the film thickness (52 nm).

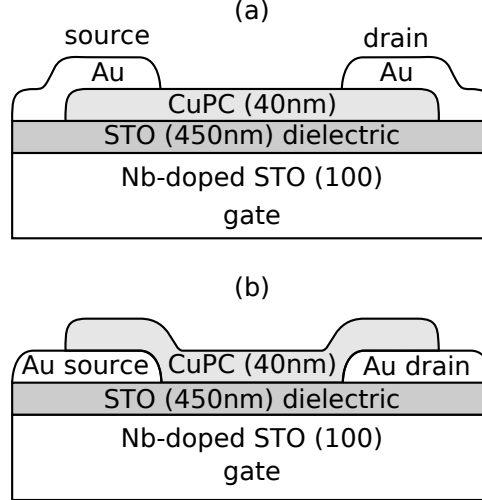
### 3.2. CuPc growth

The organic semiconductor as active layer was prepared by organic molecular beam deposition in an UHV chamber with base pressure of  $10^{-10}$  mbar. The source material was commercial CuPc and it was used without further purification. The deposition rates were kept low, between 0.4 and 0.02 nm/min. CuPc growth was studied at different substrate temperatures on  $\alpha\text{-Al}_2\text{O}_3$  (100) and  $\text{SrTiO}_3$  (100). No difference in growth behavior between these different substrates could be observed. In contrast to this the substrate temperature had a strong impact on the growth, as observed by X-ray diffraction. The temperature influence was studied in the range from room temperature to  $140^\circ\text{C}$ . The films changed with increasing substrate temperature from smooth, with small angle oscillations and only a small Bragg peak to higher crystallinity, with a larger Bragg peak and a rougher surface with few or no small angle oscillations. A selection of Bragg scans is shown in Fig. 2 for films grown on  $\alpha\text{-Al}_2\text{O}_3$  (100). The Bragg peaks were detected for all films and substrates at an angle of  $2\theta = 6.8^\circ$  which corresponds to a distance between molecular planes of 1.3 nm. The Bragg peak is in agreement with the (200) plane of the  $\alpha$ -phase of CuPc. The  $\alpha$ -phase is frequently reported for vacuum deposition of CuPc at moderate substrate temperatures [17], while the  $\beta$ -phase can be found at high substrate temperatures or deposition rates [18]. In the  $\alpha$ -phase the molecules are oriented close to edge-on with respect to the substrate. For the field-effect transistors prepared in this study an intermediate substrate temperature of  $85^\circ\text{C}$  was chosen. This temperature was selected to balance the somewhat conflicting requirements of high crystallinity and layer smoothness.

Field-effect transistors in thin film geometry with CuPc as active layer and  $\text{SrTiO}_3$  as dielectric were prepared in-situ on (100) Nb doped  $\text{SrTiO}_3$  substrates in bottom

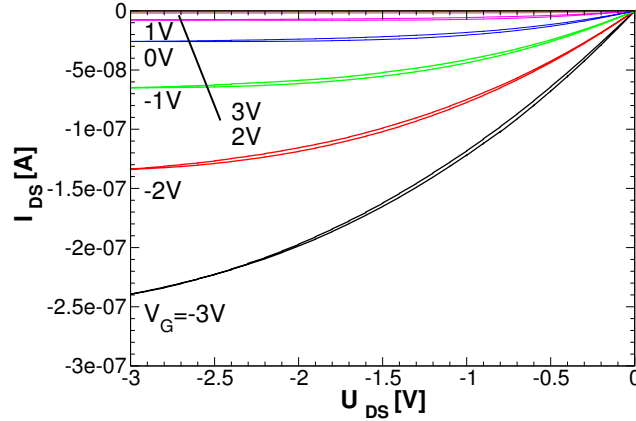


**Figure 2.** (Color online) Small angle X-ray diffraction pattern of the CuPc thin films prepared in the OMBD chamber on  $\alpha$ - $\text{Al}_2\text{O}_3$  substrates. The films were deposited on substrates at different temperatures. The film prepared at 50 °C showed pronounced Kiessig fringes but only a small Bragg peak. It was observed that this changed with higher substrate temperature - the Kiessig fringes disappeared in favor of Laue oscillations. The inset shows the corresponding rocking curves. The width (FWHM) of the rocking curve from film 009 was 0.038. Deposition time was 2 h for all films. Effusion cell temperatures were 355 °C for film 007, 350 °C for film 008 and 360 °C for film 009.



**Figure 3.** Schematic drawing of a top contact (a) and bottom contact (b) thin film transistor with bottom gate geometry. The bottom gate is realized by a conducting substrate, here Nb doped  $\text{SrTiO}_3$ , with the dielectric layer grown on top. With the use of shadow masks both top and bottom contact devices can be realized by altering the deposition order of contact and active layer deposition.

gate geometry. The source and drain electrodes were made of a 30 nm gold layer by evaporation through shadow masks. Transistors were prepared in bottom contact (contact preparation before active layer) and top contact (contact preparation after active layer) geometry as sketched in Fig. 3. The channel length was 20  $\mu\text{m}$  and the



**Figure 4.** Current voltage characteristic of a CuPc FET with  $\text{SrTiO}_3$  as dielectric layer. The "on" current at  $-3$  V source drain and  $-3$  V gate voltage was  $2.4 \cdot 10^{-7}$  A. The "off" current at  $-3$  V source drain voltage and  $0$  V gate voltage was  $2.5 \cdot 10^{-8}$  A and was further suppressed to  $3.5 \cdot 10^{-10}$  A with a gate voltage of  $3$  V. The on/off ratio was about  $10^3$ .

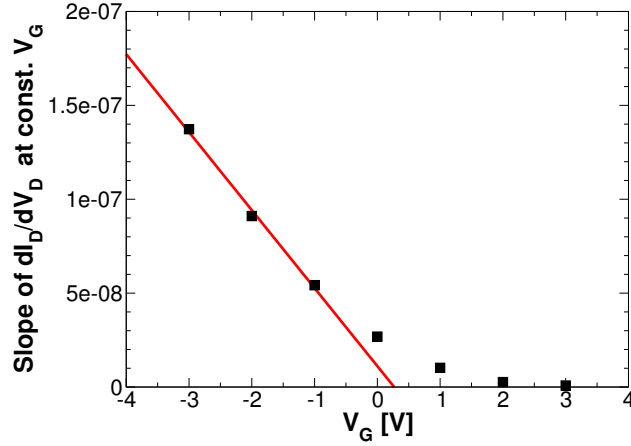
channel width was  $1$  mm. The shadow masks had a four-segment arrangement, so that there were always four (identical) transistors prepared, one in each sector of the substrate.

#### 4. Results

When measured, the four FETs on one substrate showed comparable results. The dielectric layer was characterized and  $I - V$  and transfer characteristics were measured ex-situ at room temperature.

The dielectric constant of the dielectric layer was calculated from the capacitance of the electrodes. The values obtained for  $\kappa$  from the transistors with  $\text{SrTiO}_3$  as the dielectric layer were typically around  $180$  to  $200$  and the dielectric could usually withstand voltages of about  $3$  V which corresponds to a breakdown voltage of about  $700 \text{ kV cm}^{-1}$  and a polarization of  $1.3 \mu\text{C cm}^{-2}$ . To calculate mobilities from the FET characteristics the capacitance per unit area was required, which was calculated from the measured capacitance and the area of the electrodes to about  $413 \text{ nF cm}^{-2}$ .

All CuPc transistors showed  $p$ -type semiconducting behavior. For all transistors only low voltages were necessary to achieve a pronounced modulation of the source drain current. The response characteristics of the transistors were measured multiple times with increasing voltages. The voltages were ramped up and down slowly and often a hysteresis was observed. The top contact transistors showed a better performance (i.e. higher mobility), possibly due to an annealing effect of the active layer during contact preparation, i. e. Au evaporation through a shadow mask. The response curve of a top contact FET is shown in Fig. 4. The transfer curves were measured for different fixed source drain voltages. The gate voltage was ramped up and down and also a hysteretic behavior was observed. A hysteresis behavior in organic FETs is not



**Figure 5.** This plot is used to determine the mobility in the linear regime from the response curve. The slopes of the drain current over the drain voltage  $dI_D/dV_D$  as a function of the gate voltage  $V_G \gg V_D$  (linear regime) are plotted. From the linear fit the threshold voltage was estimated by the x-axis intercept to  $V_T = 0.27$  V and the mobility was derived from the slope to  $\mu = 1.5 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$ .

uncommon and usually related to trapped charges [19].

For positive gate voltages the conductivity was suppressed and the drain current decreased below the zero gate voltage current, which can be interpreted as a depletion behavior. Saturation was hardly obtained for drain currents exceeding the gate voltage. This indicates a negative build in zero (threshold) voltage which biased the transistor. This FET had a on/off ratio of about  $10^3$ , which is comparable to literature results [15]. The mobility of the transistors can be obtained in different ways. From the current voltage curve the mobility can be calculated in the saturation regime by [20, 21]

$$\mu = \left( \frac{\partial \sqrt{I_D}}{\partial V_G} \right)^2 \cdot \frac{2L}{C_I W}, \quad (1)$$

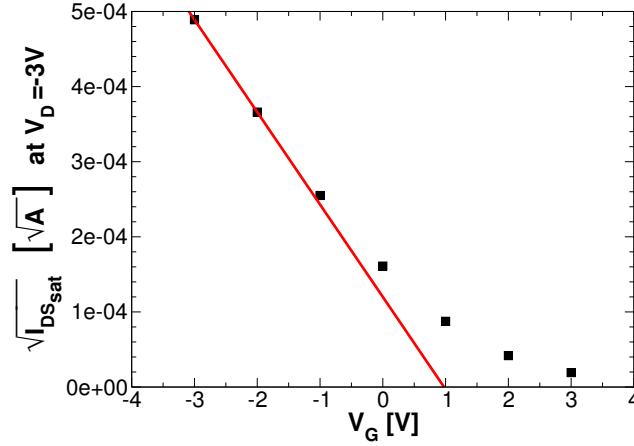
where  $L$  is the channel length,  $W$  is the channel width,  $C_I$  is the capacitance per unit area of the gate insulator,  $I_D$  is the drain current and  $V_G$  is the gate voltage. In the linear regime the mobility is obtained from the transfer curve by [20, 21]

$$\mu = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{W C_I V_D} \quad (2)$$

or from the slope of a plot, where the slopes of the response curves in the linear regime at constant gate voltage are plotted over gate voltage by [20, 21]

$$\mu = \frac{\partial I_D}{\partial V_D} \cdot \frac{L}{W C_I (V_G - V_T)}, \quad (3)$$

where  $V_D$  is the drain and  $V_T$  is the threshold voltage. The mobility obtained in the linear regime was derived from transfer curves to  $\mu = 1.8 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$ . Additionally, the mobility was determined from the slopes of the response curves for small drain voltages. A plot of the derived slopes is presented in Fig. 5. From a fit to these values a mobility of  $\mu = 1.5 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$  and a threshold voltage of  $V_T = 0.27$  V was calculated.



**Figure 6.** Plot to determine the mobility in the saturation regime from the square root of the saturation current at  $V_D = -3$  V as a function of the gate voltage. From a fit at the highest gate voltage the mobility was obtained to  $\mu = 1.1 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$  and the threshold voltage to  $V_T = 0.98$  V.

The mobility was also extracted from the saturation current as depicted in Fig. 6. The currents at  $V_D = -3$  V were obtained from the response curves from Fig. 4. The square roots of these currents were then plotted over the gate voltage and from the slope the mobility was calculated to  $\mu = 1.1 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$  and the threshold voltage to  $V_T = 0.98$  V. The plot showed the typical increase in slope towards higher gate voltages [21].

## 5. Conclusions

In summary, FETs with  $\text{SrTiO}_3$  as dielectric and CuPc as semiconductor were prepared in-situ. The values derived for mobility in the linear and the saturation regime were in good agreement and amounted to  $\mu = 1.5 \cdot 10^{-3} \text{ cm}^2/\text{Vs}$ . These mobilities were obtained without optimization of the CuPc layer with respect to transport properties. In the literature the highest mobilities of about  $\mu = 1.5$  to  $2.0 \cdot 10^{-2} \text{ cm}^2/\text{Vs}$  were reported for a substrate temperature of  $125^\circ\text{C}$  by Bao *et al.* [1] using a  $\text{SiO}_2$  dielectric and  $150^\circ\text{C}$  by Okuda *et al.* [15] using a  $\text{SiO}_2$  and a high-permittivity  $\text{PbZr}_{0.5}\text{Ti}_{0.5}\text{O}_3$  (PZT) insulator. Both groups report a dramatic field effect mobility increase with substrate temperature, in conjunction with higher crystalline order. At even higher substrate temperatures, the field effect mobilities decreased again, which was attributed to gaps between large non-space-filling crystals. Our field-effect mobility is well in agreement with the mobilities obtained by Bao *et al.* on  $\text{SiO}_2$  at a substrate temperature of  $85^\circ\text{C}$ . The on/off ratio ( $10^3$ ) is comparable to the PZT devices, but lower than the best  $\text{SiO}_2$  FETs ( $10^5$ ). The driving voltages (3 V) are also comparable to the PZT devices (2 V) and much lower than the  $\text{SiO}_2$  FETs (100 V). These results show that organic transistors with low driving voltages can be realized with a  $\text{SrTiO}_3$  dielectric. Further optimization of the  $\text{SrTiO}_3$  insulator is required to fully utilize its potential to achieve



high polarizations and enable organic MTFETs, as well as basic research on the effects of large induced interface charges in organic charge transfer materials [22, 23].

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## References

- [1] Z. Bao, A. J. Lovinger, and A. Dodabalapur, J. Appl. Phys. 69 (1996) 3066
- [2] S. F. Nelson, Y. Lin, D. J. Gundlach, and T. N. Jackson, Appl. Phys. Lett. 72 (1998) 1854
- [3] J. B. Torrance, Accounts of Chemical Research 12 (1979) 79
- [4] I. Sarkar, M. Laux, J. Demokritova, A. Ruffing, S. Mathias, J. Wei, V. Solovyeva, M. Rudloff, S. S. Naghavi, C. Felser, M. Huth, and M. Aeschlimann, Appl. Phys. Lett. 97 (2010) 111906
- [5] V. Solovyeva and M. Huth, Synth. Met. in print (2011)
- [6] C. Zhou, D. M. Newns, J. A. Misewich, and P. C. Pattnaik, Appl. Phys. Lett. 70 (1997) 598
- [7] N. Mott, *Metal-Insulator Transitions*, Taylor & Francis, London, 1990
- [8] D. M. Newns, J. A. Misewich, C. C. Tsuei, A. Gupta, B. A. Scott, and A. Schrott, Appl. Phys. Lett. 73 (1998) 780
- [9] A. Walkenhorst, C. Doughty, X. X. Xi, S. N. Mao, Q. Li, T. Venkatesan, and R. Ramesh, Appl. Phys. Lett. 60 (1992) 1744
- [10] C. H. Ahn, J.-M. Triscone, and J. Mannhart, Nature 424 (2003) 1015
- [11] H.-M. Christen, J. Mannhart, E. J. Williams, and C. Gerber, Phys. Rev. B 49 (1994) 12095
- [12] H. Tabata, H. Tanaka, and T. Kawai, Appl. Phys. Lett. 65 (1994) 1970
- [13] J. H. Haeni, P. Irvin, W. Chang, R. Uecker, P. Reiche, Y. L. Li, S. Choudhury, W. Tian, M. E. Hawley, B. Craigo, A. K. Tagantsev, X. Q. Pan, S. K. Streiffer, L. Q. Chen, S. W. Kirchoefer, J. Levy, and D. G. Schlom, Nature 430 (2004) 758
- [14] T. Tomio, H. Miki, H. Tabata, T. Kawai, and S. Kawai, J. Appl. Phys. 76 (1994) 5886
- [15] T. Okuda, S. Shintosh, and N. Terada, J. Appl. Phys. 96 (2004) 3586
- [16] L. S.-J. Peng, X. X. Xi, B. H. Moeckly, and S. P. Alpay, Appl. Phys. Lett. 83 (2003) 4592
- [17] L. Lozzi, S. Santucci, S. L. Rosa, B. Delley, and S. Picozzi, J. Chem. Phys. 121 (2004) 1883
- [18] O. Berger, W. Fischer, B. Adolphi, S. Tierbach, V. Melev, and J. Schreiber, J. Mat. Sci. 11 (2000) 331
- [19] M. Mas-Torrent, M. Durkut, P. Hadley, X. Ribas, and C. Rovira, J. Am. Chem. Soc. 126 (2004) 984
- [20] G. Horowitz, J. Adv. Mat. 10 (1998) 365
- [21] C. R. Newman, C. D. Frisbie, D. A. da Silva Filho, J. Bredas, P. C. Ewbank, and K. R. Mann, Chem. Mater. 16 (2004) 4436
- [22] V. Solovyeva, K. Keller, and M. Huth, Thin Solid Films 517 (2009) 6671
- [23] K. Medjanik, S. Perkert, S. Naghavi, M. Rudloff, V. Solovyeva, D. Chercka, M. Huth, S. A. Nepijko, T. Methfessel, C. Felser, M. Baumgarten, K. Müllen, H. J. Elmers, and G. Schönhense, Phys. Rev. B 82 (2010) 245419